ELEC 422 / 527, VLSI Systems Design
Course Description, Spring 2020

Instructor:
Joseph Cavallaro, Duncan Hall (DCH) 3042, x4719, cavallar@rice.edu
Office hours: T, Th 2:30 - 4:00 pm after class

Course Schedule:
Credits: 3
Class Contact hours: Day & Time: T, Th 1:00 - 2:15 pm, Location: AEL A116 lab.
Additional meetings to discuss group project progress will be arranged.

Grading:
Six Homework assignments during the semester. (30%) (Independent work under the Honor System).
Final Exam (Take-home, Honor System, closed book) (20%).

Group Project (Groups of 2 or 3) to be fabricated by MOSIS (50% total).
a. Group Project Presentation, Design Reviews and Class Participation (10%).
b. Group Project Report (Due last day of class) (10%)
c. Group Project Mask Design (CIF/GDSII) File simulated and integrated into padframe ready for MOSIS submission (Due last day of class to meet MOSIS deadline) (30%).

Class participation:
Students are expected to attend both class lecture and project group meetings and are encouraged to ask questions throughout the semester.

Course Textbook (Required):
Weste and Harris "CMOS VLSI Design: A Circuits and Systems Perspective" Third Edition, Addison-Wesley, 2005. ISBN: 0-321-14901-7
http://www.amazon.com/CMOS-VLSI-Design-Circuits-Perspective/dp/0321149017/ref=mt_hardcover?_encoding=UTF8&me=

We plan to use the Third Edition this year instead of the Fourth Edition.

Course Description:
A study of VLSI technology and design. MOS devices, characteristics and fabrication. Logic design and implementation. VLSI design methodology, circuit simulation and verification.

Prerequisites:
ELEC 326 or a course on digital logic design.

Course Status:
A selected Specialization Elective for majors in Electrical and Computer Engineering and Computer Science

Course Websites:
We will be using Canvas for the assignments and lab projects and announcements. Also class notes and readings will be posted to the Canvas site. This syllabus will also be posted to the external Web Page: https://www.clear.rice.edu/elec422/

Course Goals and Objectives:

At the end of the course, students should be able to understand and analyze the hardware components of a modern application specific integrated circuit (ASIC) and very large scale integration (VLSI) technology. They should be able to apply this knowledge to create hardware elements to enable new applications. Also, they should be able to evaluate the efficiency and effectiveness of their solutions and remember the basic structure of hardware components and the basic syntax of hardware description languages and computer aided design (CAD) tools.

Course Outcomes: Related to ABET Criterion 3 a through k:

The relationships to eleven criteria are listed with 1, 2, and 3. (with 3 as most related.)

a	An ability to apply knowledge of mathematics, science, and engineering.	3
b	An ability to design and conduct experiments, as well as to analyze and interpret data.	2
c	An ability to design a system, component, or process to meet desired needs.	3
d	An ability to function on multi-disciplinary teams.	
e	An ability to identify, formulate, and solve engineering problems.	2
f	An understanding of professional and ethical responsibility.	
g	An ability to communicate effectively.	2
h	The broad education necessary to understand the impact of engineering solutions in a global and societal context.	
i	A recognition of the need for, and an ability to engage in life-long learning.	
j	A knowledge of contemporary issues.	
k	An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.	3

Course Topics:
The course topics will include: Logic Design and Simulation.
"Stick" Diagrams. Hierarchical Layout Methodology.
Mask Level Computer-Aided Design Tools: irsim, magic, spice...
System Level Tools including Verilog and Modelsim.
Higher Level Design tools: Synopsys Design Compiler, Cadence Virtuoso and SoC Encounter (EDI), Xilinx Vivado HLS, Xilinx FPGA (AL A116 Lab).
State Machine Design and Programmable Logic Arrays.
System Routing, Clock Distribution, and I/O.
Design for Testability; Fault Tolerance. CMOS Processing.
MOSIS Scalable CMOS Design; 0.5 micron nwell process.

New for 2020:
We will be using again the CLEAR (Curricular Linux Environment At Rice) Linux cluster in 2020. Some computer aided design (CAD) tools will be Windows based and most will be on the CLEAR Linux server and require X terminal software such as MobaXterm from Windows or XQuartz from Macintosh. The Abercrombie Labs AEL A116 lab has 15 Windows computers with MobaXterm installed for access to CLEAR. This is the fifth year of ELEC 422 / 527 as ELEC 422 returned in 2016. We will study a broad range of CAD tools for ASIC design and perhaps utilize FPGA's for initial verification and chip testing. We plan to introduce System Verilog for verification in addition to Verilog.

Honor Code Policy:
General Assignments: When working in groups for labs and projects, your group counts as a single individual for this policy, and your group receives a single score. You may use your text, course notes, and any other reference material (that is not a solution). You may discuss problems, general strategies, or algorithms with other people (in the course or not). When partnering, you should understand and be able to recreate any part of the solutions on your own. For all assignments, you may NOT use solutions from past classes or found on the web. You may not obtain code from anyone (in the course or not), aside from code provided as part of the course.

Exam Honor Code: Complete all exams individually.

Homework Honor Code: Complete homework assignments individually. Please list your name on the submitted solution. Solutions submitted after the date and time specified will receive no credit. You may freely use the 2020 course notes, the course textbook, or course handouts for the assignments. Students may discuss and compare ideas on the homework assignments, but each student must write up solutions individually without resort to copying. That is, students must not create submissions together; students may discuss problems but may not actually write up their assignments together. You should also not refer to solutions posted on the web or from previous years' classes. Clearly state any assumptions that you make in order to solve the problems and show all your work.

Students with Disabilities:
Any student with a disability requiring accommodations in this course is encouraged to contact the instructor after class or during office hours. Additionally, students will need to contact Disability Support Services in the Ley Student Center.

Updates to the Course:
Information contained in this course syllabus, other than the absence policies, may be subject to change with reasonable advance notice as appropriate.

ELEC 527 Additional Course Work:
Graduate students in ELEC 527 will have additional project/report work. This will typically be a research literature survey and analysis report analyzing a current research topic in VLSI Design. The report will be in a 6 page IEEE conference paper format.

Prepared by: Joseph Cavallaro Date: December 28, 2019